LCP1531

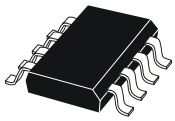
Programmable transient voltage suppressor for SLIC protection

Features

- Dual programmable transient suppressor
- Wide negative firing voltage range: V_{MGL} = -150 V max.
- Low dynamic switching voltages: V_{FP} and V_{DGL}
- Low gate triggering current: I_{GT} = 5 mA max
- Peak pulse current: I_{PP} = 37.5 A (5/310 µs)
- Holding current: I_H = 150 mA min
- Low space consuming package

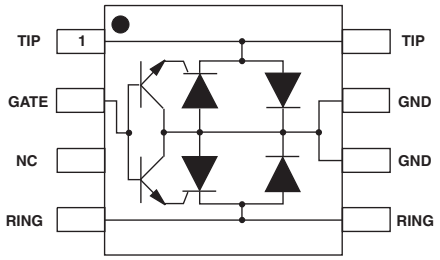
Benefits

Trisils™ are not subject to ageing and provide a fail-safe mode in short circuit for better protection. They are used to help equipment to meet various standards such as YDT695, and ITU-T K20/21. Trisils are UL94 V0 resin approved and are UL497B approved [file: E136224]).



SO-8

Figure 1. LCP1531 functional diagram



Description

These devices are ideally suited to meet the protection requirement of VoIP SLICs located in next generation residential gateways. They can be used for protecting any ringing SLIC since they meet the protection standard requirements.

Positive overvoltages are clamped by 2 diodes. Negative surges are suppressed by 2 thyristors, their breakdown voltage being referenced to $-V_{BAT}$ through the gate.

These components present a very low gate triggering current (I_{GT}) to reduce the current consumption on printed circuit board during the firing phase.

TM: Trisil is a trademark of STMicroelectronics

1 Characteristics

Table 1. Compliance with the following standards

Standard	Peak surge voltage (V)	Voltage waveform	Required peak current (A)	Current waveform	Minimum serial resistor to meet standard (Ω)
YDT695, ITU-T-K20/K21	1500	10/700 µs	37.5	5/310 µs	0
ITU-T-K20 (IEC 61000-4-2)	8000 15000	1-60 ns	ESD contact discharge ESD air discharge		0 0

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{th(j-a)}$	Junction to ambient	120	°C/W

Table 3. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter
I_{GT}	Gate triggering current
I_H	Holding current
I_{RM}	Reverse leakage current LINE / GND
I_{RG}	Reverse leakage current GATE / LINE
V_{RM}	Reverse voltage LINE / GND
V_{GT}	Gate triggering voltage
V_F	Forward drop voltage LINE / GND
V_{FP}	Peak forward voltage LINE / GND
V_{DGL}	Dynamic switching voltage GATE / LINE
V_{RG}	Reverse voltage GATE / LINE
C	Capacitance LINE / GND

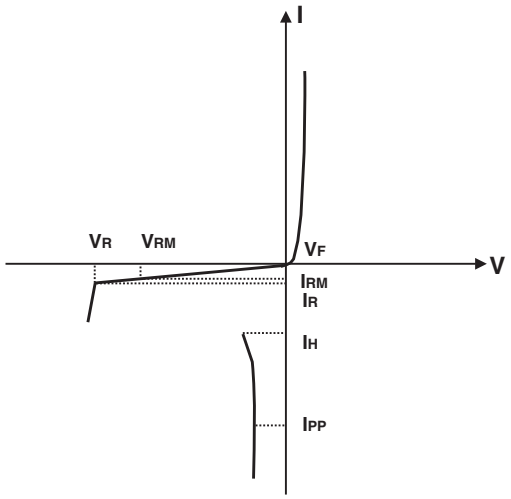


Table 4. Absolute ratings (T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current	5/310 µs	37.5	A
I_{TSM}	Non-repetitive surge peak on-state current (50 Hz sinusoidal)	t = 20 ms t = 200 ms t = 1 s	16 9 6	A
I_{GSM}	Maximum gate current (50 Hz sinusoidal)	t = 10 ms	2	A
V_{MLG} V_{MGL}	Maximum voltage LINE/GND Maximum voltage GATE/LINE		-150 -150	V
T_{stg} T_j	Storage temperature range Maximum junction temperature		-55 to +150 150	°C
T_L	Maximum lead temperature for soldering during 10 s.		260	°C

Table 5. Repetitive peak pulse current

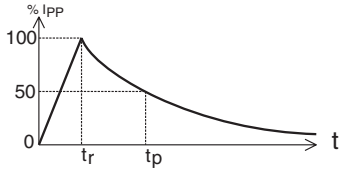
Symbol	Definition	Example	
t_r	Rise time (µs)	Pulse waveform 5/310 µs: t_r = 5 µs t_p = 310 µs	
t_p	Pulse duration (µs)		

Table 6. Parameters related to the diode LINE / GND (T_{amb} = 25 °C)

Symbol	Test conditions			Max	Unit
V_F	I_F = 5 A		t = 500 µs	3	V
V_{FP}(1)	10/700 µs	V_{PP} = 1.5 kV	R_S = 15 Ω	5	V

1. see test circuit for V_{FP}; R_S is the protection resistor located on the line card.

Table 7. Parameters related to the protection thyristors (T_{amb} = 25 °C)

Symbol	Test conditions	Min	Max	Unit
I_{GT}	$V_{GND\ /\ LINE}$ = -48 V	0.1	5	mA
I_H	V_{GATE} = -48 V(1)	150		mA
I_{RG}	V_{RG} = -75 V		5	µA
V_{DGL}	V_{GATE} = -48 V(2) 10/700 µs V_{PP} = 1.5 kV R_S = 15 Ω I_{PP} = 27.5 A		7	V

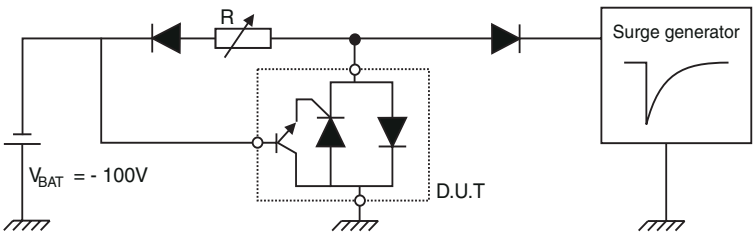
1. See functional holding current (I_H) test circuit (*Figure 2*).
2. see test circuit for V_{DGL} (*Figure 3*.) The oscillations with a time duration lower than 50 ns are not taken into account.

Table 8. Parameters related to diode and protection thyristors (T_{amb} = 25 °C, unless otherwise specified)

Symbol	Test conditions		Typ	Max	Unit
I_{RM}	$V_{GATE\ /\ LINE}$ = -1 V V_{RM} = -75 V	T_j = 25 °C		5	µA
C	V_R = 50 V bias, V_{RMS} = 1 V, F = 1 MHz V_R = 2 V bias, V_{RMS} = 1 V, F = 1 MHz		15 35		pF

2 Technical information

Figure 2. Functional holding current (I_H) test circuit: go - no go test



This is a go - no go test which allows confirmation of the holding current (I_H) level in a functional test circuit.

TEST PROCEDURE:
- Adjust the current level at the I_H value by short circuiting the D.U.T.
- Fire the D.U.T. with a surge current: I_{PP} = 10A, 10/1000µs
- The D.U.T. will come back to the off-state within a duration of 50ms max.

Figure 3. Test circuit for V_{FP} and V_{DGL} parameters

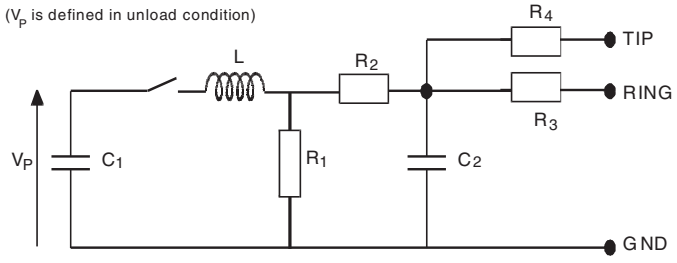


Table 9. Components and values for test circuit in *Figure 3*

Pulse (µs)		V_p (V)	C_1 (µF)	C_2 (nF)	L (µH)	R_1 (Ω)	R_2 (Ω)	R_3 (Ω)	R_4 (Ω)	I_{PP} (A)	R_s (Ω)
t_r	t_p										
10	700	1500	20	200	0	50	15	25	25	30	10

Figure 4. LCP1531 concept behavior

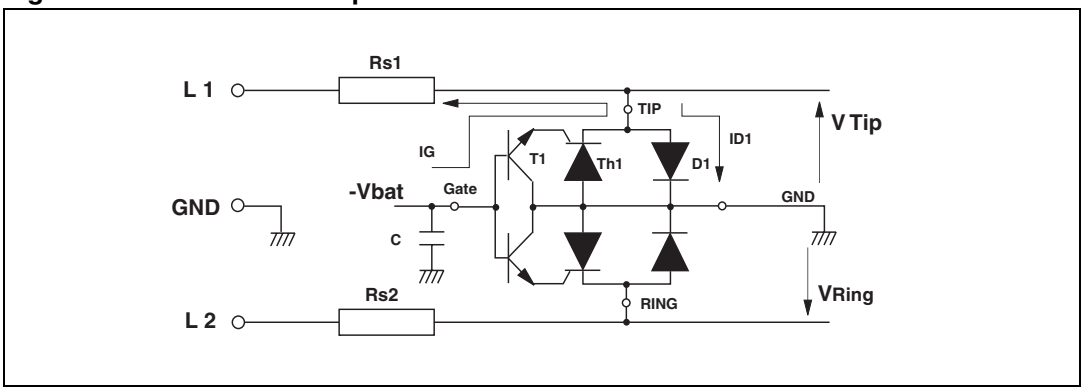


Figure 4. shows the classical protection circuit using the LCP1531 crowbar concept. This topology has been developed to protect the new high voltage SLICs. It allows to program the negative firing threshold while the positive clamping value is fixed at GND.

When a negative surge occurs on one wire (L1 for example) a current IG flows through the base of the transistor T1 and then injects a current in the gate of the thyristor Th1. Th1 fires and all the surge current flows through the ground. After the surge when the current flowing through Th1 becomes less negative than the holding current IH, then Th1 switches off.

When a positive surge occurs on one wire (L1 for example) the diode D1 conducts and the surge current flows through the ground.

Figure 5. Example of PCB layout based on LCP1531 protection

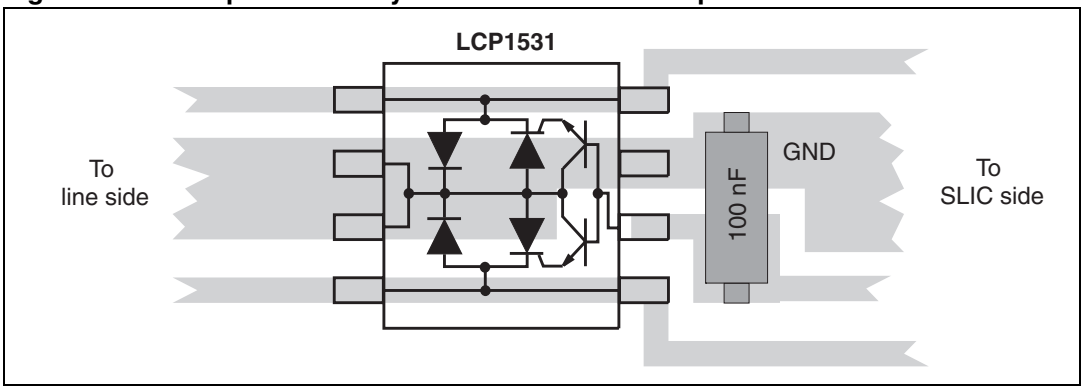


Figure 5. shows the classical PCB layout used to optimize line protection.

The capacitor C is used to speed up the crowbar structure firing during the fast surge edges.

This allows to minimize the dynamical breakover voltage at the SLIC Tip and Ring inputs during fast strikes. Note that this capacitor is generally present around the SLIC - V_{bat} pin.

So to be efficient it has to be as close as possible from the LCP1531 Gate pin and from the reference ground track (or plan) (see *Figure 5.*). The optimized value for C is 100 nF.

The series resistors Rs1 and Rs2 designed in *Figure 4.* represent the fuse resistors or the PTC which are mandatory to withstand the power contact or the power induction tests imposed by the various country standards. Taking into account this fact the actual lightning surge current flowing through the LCP1531 is equal to:

$I_{surge} = V_{surge} / (R_g + R_s)$

With:

V_{surge} = peak surge voltage imposed by the standard.

R_g = series resistor of the surge generator

R_s = series resistor of the line card (e.g. PTC)

The LCP1531 is particularly optimized for the new telecom applications such as the fiber in the loop, the WLL, the remote central office. In this case, the operating voltages are smaller than in the classical system. This makes the high voltage SLICs particularly suitable.

The schematics of *Figure 6.* gives the most frequent topology used for these applications.

Figure 6. Protection of high voltage SLIC

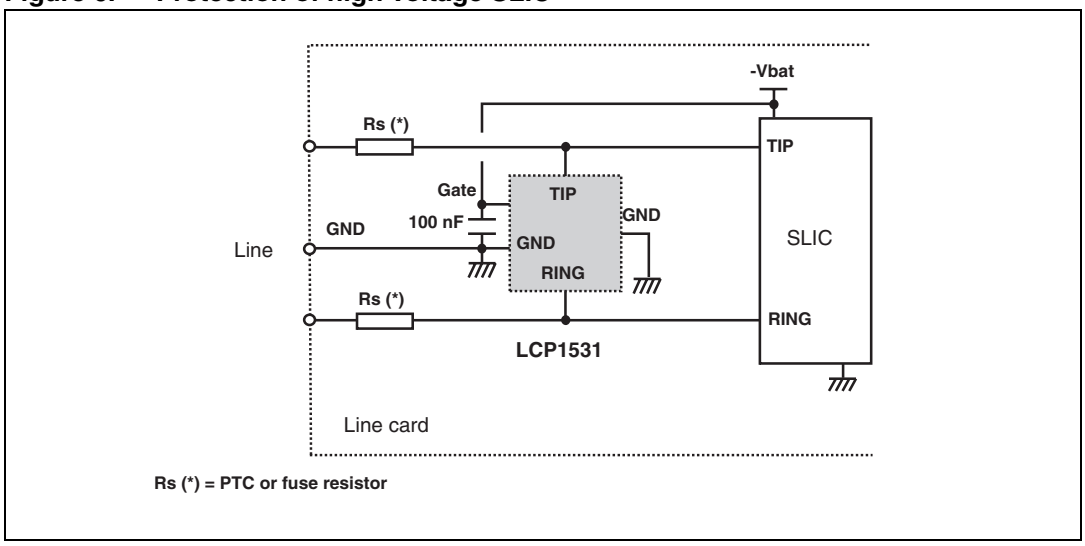


Figure 7. Surge peak current versus overload duration

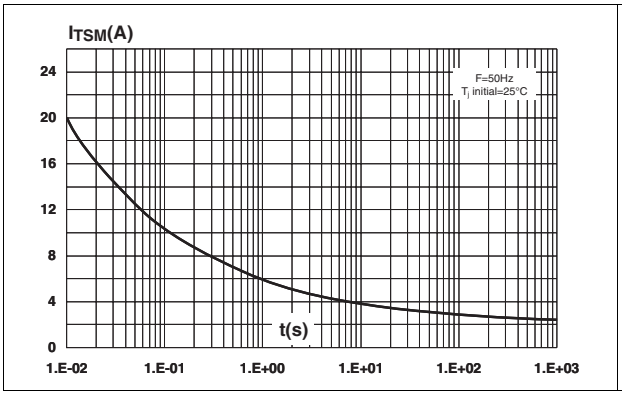
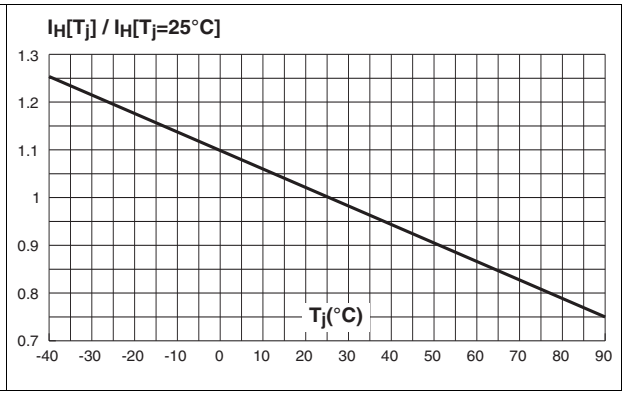


Figure 8. Relative variation of holding current versus junction temperature

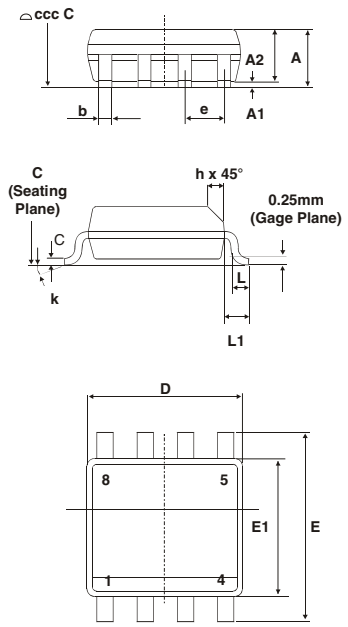


3 Package information

- Epoxy meets UL94, V0

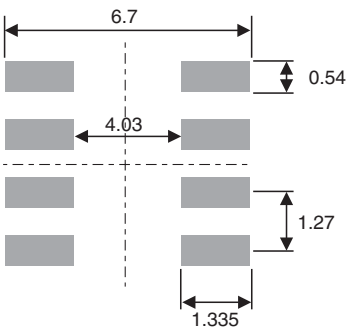
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at *www.st.com*.

Table 10. SO-8 dimensions



Ref	Dimensions					
	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A			1.75			0.069
A1	0.1		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
C	0.17		0.23	0.007		0.009
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.041	
k°	0		8	0		8
ccc			0.10			0.004

Figure 9. SO-8 footprint (dimensions in mm)



4 Ordering information

Table 11. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
LCP1531RL	CP153	SO-8	0.08 g	2500	Tape and reel

5 Revision history

Table 12. Document revision history

Date	Revision	Description of changes
23-Mar-2007	1	First issue.
10-Apr-2008	2	Reformatted for current standards. Changed gate capacitance from 220 nF to 100 nF.